In the Claims:

Please cancel claims 1-76 without any disclaimer or a prejudice, add new claims 77-96 as follows:

1-76 (Cancelled)

77. (Newly Added) A shift register in which multiple stages are connected one after another to each other, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

each of the multiple stages comprising:

a pull-up section for providing a corresponding one of the first and second clock signals to an output terminal;

a pull-up driving section coupled to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal and turning off the pull-up section in response to a front edge of an output signal of one of next stages;

a pull-down section for providing a first power voltage to the output terminal;

and

a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to the front edge of the input signal and turning on the pull-down section in response to the front edge of the output signal of one of the next stages.

78. (Newly Added) The shift register of claim 77, wherein each of the multiple stages further comprises a floating preventing section coupled to the input node of the pull-down section, wherein the floating preventing section provides a second power voltage to the input node of the pull-down section to prevent the input node of the pull-down section from being floated.

79. (Newly Added) A display device comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages coupled one after another to each other, the multiple stages sequentially selecting the multiple gate lines using an output signal of each stage, and the multiple stages having odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a control terminal coupled to an output terminal of one of next stages;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up section coupled between the clock terminal and the output terminal, for pulling-up the corresponding gate line during a duty period of the clock signal of when the pull-up section is turned on;

a pull-down section coupled between the output terminal and a first power voltage, for pulling-down the corresponding gate line when the pull-down section is turned on;

a pull-up driving section coupled to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up section in response to a front edge of a control signal supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to the front edge of the input signal and turning on the pull-down section in response to the front edge of the control signal.

80. (Newly Added) The display device of claim 79, wherein each of the multiple stages further comprises a floating preventing section coupled between the input node of the pull-down section and a second power voltage, for connecting the second power voltage to the input node of the pull-down section to prevent the input node of the pull-down section from being floated.

81. (Newly Added) An display device comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit

comprising multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

wherein the data driving circuit comprises multiple data line blocks and a shift register,

wherein each of the data line blocks comprises multiple driving transistors each of which drain and source are respectively coupled between a data input terminal and the data line and gate is commonly coupled to a block selection terminal,

wherein the shift register comprises multiple stages coupled one after another to each other, the multiple stages sequentially selecting the multiple data line blocks using an output signal of each of the multiple stages, and the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a block selection terminal of a corresponding data line block;

a control terminal coupled to an output terminal of one of next stages;

a clock terminal into which a corresponding clock signal is input;

a pull-up section coupled between the clock terminal and the output terminal, for pulling-up the corresponding gate lien during a duty period of the clock signal of when the pull-up section is turned on;

a pull-down section coupled between the output terminal and a first power voltage, for pulling-down the corresponding gate line using the first power voltage when the pull-down section is turned on;

a pull-up driving section coupled to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up section in response to a front edge of a control signal supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to the front edge of the input signal and turning on the pull-down section in response to the front edge of the control signal.

82. (Newly Added) The display device of claim 81, wherein said each of the multiple stages comprises a floating preventing section coupled between the input node of the pull-down section and a second power voltage, the input node of the pull-down section being coupled to the second power voltage, for preventing the input node of the pull-down section from being floated.

83. (Newly Added) An LCD having an LCD module in which a liquid crystal is interposed between a lower substrate and an upper substrate, the LCD comprising:

a display cell array circuit formed on the lower substrate, comprising multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

a gate driving circuit formed on the lower substrate and comprising a first shift register comprising multiple stages coupled one after another to each other, the first shift register sequentially selecting the multiple gate lines using an output signal of each stage;

a data driving circuit formed on the lower substrate and comprising multiple data line blocks and a second shift register, each of the data line blocks comprising multiple driving transistors each of which a first current electrode and a second current electrode are coupled between a data input terminal and the data line and a control electrode is commonly coupled to a block selection terminal, the second shift register comprising multiple stages coupled one after another to each other, the multiple stages sequentially selecting the multiple data line blocks using an output signal of each of the multiple stages; and

a flexible printed circuit board on which an integral control and data driving chip is mounted, for providing a control signal and a data signal to the input terminal of the gate and data driving circuits.

84. (Newly Added) A shift register in which multiple stages are coupled one after another to each other, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

each of the multiple stages comprising:

a pull-up section for providing a corresponding one of the first and second clock signals to an output terminal;

a pull-up driving section, coupled to an input node of the pull-up section, for charging a capacitor in response to a front edge of an input signal to turn on the pull-up section and discharging the capacitor in response to a front edge of an output signal of one of next stages to turn off the pull-up section;

a pull-down section for providing a first power voltage to the output terminal; and

a pull-down driving section, coupled to an input node of the pull-down section and the input node of the pull-up section, for turning off the pull-down section and turning on the pull-down section in response to the front edge of the output signal of one of the next stages.

85. (Newly Added) A shift register in which multiple stages are coupled one after another to each other, the shift register sequentially outputting output signals of respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

each of the multiple stages comprising:

an NMOS pull-up transistor of which a first current electrode is coupled to a corresponding clock signal, a control electrode iscoupled to a first node, and a second current electrode is coupled to an output terminal;

an NMOS pull-down transistor of which a first current electrode is coupled to the output terminal, a control electrode is coupled to a second node and a second current electrode is coupled to a first power voltage;

a capacitor coupled between the first node and the output terminal;

a first transistor of which a first current electrode is coupled to a second power voltage, a control electrode is coupled to an input signal and a second current electrode is coupled to the first node;

a second transistor of which a first current electrode is coupled to the first node, a control electrode is coupled to an output signal of one of next stages and a second current electrode is coupled to the first power voltage;

a third transistor of which a first current electrode is coupled to the first node, a control electrode is coupled to the second node and a second current electrode is coupled to the first power voltage;

a fourth transistor of which a first current electrode and a control electrode are commonly coupled to a second power voltage and a second current electrode is coupled to the second node; and

a fifth transistor of which a first current electrode is coupled to the second node, a control electrode is coupled to the first node and a second current electrode is coupled to the first power voltage.

86. (Newly Added) A shift register including multiple stages coupled in a cascade fashion, the multiple stages sequentially outputting output signals of the respective stages, the multiple stages having odd numbered stages for receiving a first clock signal and a second clock signal having a phase different from the first clock signal at a first clock terminal and a second clock terminal of the odd numbered stages, and even numbered stages for receiving the second

clock signal and the first clock signal at a first clock terminal and a second clock terminal of the even numbered stages,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a first control terminal coupled to a second control terminal of a stage after a next stage;

a second control terminal;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up section for providing a corresponding one out of the first and second clock signals to the output terminal;

a pull-down section for providing a first power voltage to the output terminal;

a pull-up section coupled to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal and turning off the pull-up section in response to a front edge of a control signal supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section and an input node of the pull-up section, for turning off the pull-down section, and for turning on the pull-down section in response to a front edge of the output signal of the next stage.

87. (Newly Added) A display device comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages coupled in a cascade fashion, the shift register for sequentially outputting output signals of the respective stages, the multiples stages having odd numbered stages for receiving a first clock signal and a second clock signal having a phase different from the first clock signal at a first clock terminal and a second clock terminal of the odd numbered stages, and even numbered stages for receiving the second clock signal and the first clock signal at a first clock terminal and a second clock terminal of the even numbered stages,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a first control terminal coupled to a second control terminal of a stage after a next stage;

a second control terminal;

a clock terminal into which a corresponding clock signal is inputted;

a pull-up section coupled between the clock terminal and the output terminal, for turning on the corresponding gate line during a duty period of the clock signal;

a pull-down section coupled between the output terminal and a first power voltage, for pulling-down the corresponding gate line when the pull-down section is turned on;

a pull-up driving section coupled to an input node of the pull-up section, for turning on the pull-up section in response to a front edge of an input signal supplied to the input terminal and turning off the pull-up section in response to a front edge of a control signal of the stage after the next stage supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section and an input node of the pull-up section, for turning off the pull-down section and for turning on the pull-down section in response to a front edge of an output signal of the next stage.

88. (Newly Added) A shift register including multiple stages coupled in a cascade fashion, the multiple stages sequentially outputting output signals of the respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and a second clock signal having a phase different from the first clock signal,

wherein each of the multiple stages comprises:

a pull-up section for providing a corresponding one out of the first and second clock signals;

a pull-down section for providing a first power voltage to the output terminal;

a pull-down driving section coupled to an input node of the input signal and turning on the pull-down section in response to a front edge of an output signal of one of next stages; and

a pull-up driving section provided with a capacitor of which a first end is coupled to an input node of the pull-up section and a second end is coupled to the output terminal, and a discharging section for forcibly discharging the capacitor depending on an external input control signal, the pull-up driving section turning on the pull-up section by charging the capacitor in response to the front edge of the input signal and turning off the pull-up section by forcibly discharging the capacitor in response to the front edge of the output signal of one of the next stages.

89. (Newly Added) An display device comprising a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit comprising multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

the gate driving circuit comprising a shift register including multiple stages coupled in cascade fashion, the shift register sequentially selecting the multiple gate lines depending on output signals of the respective stages, the multiple stages having odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a control terminal coupled to a control terminal of one of next stages;

a clock terminal into which a corresponding clock signal is inputted;

an external input control terminal for receiving an external input control signal;

a pull-up section for providing a corresponding one out of the first and second clock signals to the output terminal;

a pull-down section for providing a first power voltage to the output terminal;

a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to a front edge of the input signal and turning on the pull-down section in response to a front edge of an output signal of one of next stages; and

a pull-up driving section provided with a capacitor of which one end is coupled to an input node of the pull-up section and the other end is coupled to the output terminal, and a discharging section for forcibly discharging the capacitor depending on the external input control signal applied to the external input control terminal, the pull-up driving section turning on the pull-up section by charging the capacitor in response to the front edge of the input signal and turning off the pull-up section by forcibly discharging the capacitor in response to the front edge of the output signal of one of the next stages.

90. (Newly Added) A shift register having a plurality of stages, the shift register sequentially outputting signals of respective stages, the stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a different phase from the first clock signal,

each of the stages comprising:

a pull-up section to provide an output terminal with a corresponding one of the first and second clock signals;

a pull-up driving section, coupled to an input node of the pull-up section, to turn on the pull-up section in response to an input signal, and to turn off the pull-up section in response to an output signal of one of next stages;

a pull-down section to provide the output terminal with a first power voltage; and

a pull-down driving section coupled to an input node of the pull-down section, to turn off the pull-down section in response to the input signal, and to turn on the pull-down section in response to the output signal of one of the next stages.

91. (Newly Added) The shift register of claim 90, wherein each of the stages further comprises a floating preventing section coupled to the input node of the pull-down section, wherein the floating preventing section provides the input node of the pull-down section with a second power voltage to prevent the input node of the pull-down section from being floated.

92. (Newly Added) A display device having a display cell array circuit, a data driving circuit and a gate driving circuit formed on a substrate, the display cell array circuit having multiple data lines and multiple gate lines, each of the display cell arrays coupled to a corresponding pair of data line and gate line,

the gate driving circuit including a shift register, the shift register having a plurality of stages, the stages sequentially selecting the multiple gate lines using an output signal of each of the stages, and the stages having odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a different phase from the first clock signal,

wherein each of the stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a control terminal coupled to an output terminal of one of next stages;

a clock terminal for receiving a corresponding clock signal;

a pull-up section coupled between the clock terminal and the output terminal to pull up the corresponding gate line during an active period of the clock signal when the pull-up section turns on;

a pull-down section coupled between the output terminal and a first power voltage to pull down the corresponding gate line when the pull-down section turns on;

a pull-up driving section coupled to an input node of the pull-up section to turn on the pull-up section in response to an input signal supplied to the input terminal, and to turn off the pull-up section in response to a control signal supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section to turn off the pull-down section in response to the input signal, and to turn on the pull-down section in response to the control signal.

93. (Newly Added) The display device of claim 92, wherein each of the stages further comprises a floating preventing section coupled between the input node of the pull-down section and a second power voltage, the floating preventing section providing the input node of the pull-down section with the second power voltage to prevent the input node of the pull-down section from being floated.

94. (Newly Added) A shift register including multiple stages, the multiple stages sequentially outputting output signals of respective stages, the multiple stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a phase different from the first clock signal,

wherein each of the multiple stages comprises:

an input terminal coupled to an output terminal of one of previous stages;

an output terminal coupled to a corresponding gate line;

a control terminal coupled to an output terminal of one of next stages;

a clock terminal into which a corresponding clock signal out of the first and second clock signals is inputted;

a pull-up section coupled between the clock terminal and the output terminal, for providing the corresponding clock signal to the output terminal when the pull-up section turns on;

a pull-down section coupled between the output terminal and a first power voltage, for providing the first power voltage to the output terminal when the pull-down section turns on;

a pull-up driving section coupled to an input node of the pull-up section, for turning on the pull-up section in response to an input signal supplied to the input terminal, and for turning off the pull-up section in response to a control signal supplied to the control terminal; and

a pull-down driving section coupled to an input node of the pull-down section, for turning off the pull-down section in response to the input signal, and turning on the pull-down section in response to the control signal.

95. (Newly Added) The shift register of claim 94, wherein each of the multiple stages further comprises a floating preventing section coupled between the input node of the pull-down section and a second power voltage, for providing the input node of the pull-down section with the second power voltage to prevent the input node of the pull-down section from being floated.

96. (Newly Added) A substrate on which a shift register is formed, the shift register having a plurality of stages and sequentially outputting output signals of respective stages, the stages including odd numbered stages for receiving a first clock signal and even numbered stages for receiving a second clock signal having a different phase from the first clock signal,

each of the stages comprising:

a pull-up section to provide an output terminal with a corresponding one of the first and second clock signals;

a pull-up driving section, coupled to an input node of the pull-up section, to turn on the pull-up section in response to an input signal, and to turn off the pull-up section in response to an output signal of one of next stages;

a pull-down section to provide the output terminal with a first power voltage; and

a pull-down driving section coupled to an input node of the pull-down section, to turn off the pull-down section in response to the input signal, and to turn on the pull-down section in response to the output signal of one of the next stages.